Interconnection Standard Grid-Support Function Evaluations using an Automated Hardware-in-the-Loop Testbed

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Abstract — Grid operators are increasingly turning to new advanced grid-support functions in distributed energy resources (DER) to assist with distribution circuit voltage regulation, bulk system frequency control, and power system protection. While these functions have been deployed in Europe for years, the United States is in the process of adding them to state and national interconnection standards. The U.S. certification standard, Underwriters Laboratories (UL) 1741, was revised in September 2016 to add test procedures for multiple grid-support functions. Unlike the previous version of UL 1741, the test protocol now requires hundreds of permutations of operational conditions to assess the grid-support functions. Therefore, to efficiently execute the test procedures, an automated test platform must be employed. Sandia National Laboratories, SunSpec Alliance, and growing community of collaborators have undertaken a multi-year effort to create an open-source System Validation Platform (SVP) which automates DER interconnection and interoperability test procedures by communicating with grid simulators, PV simulators, data acquisition systems, and interoperable equipment under test (EUT). However, the power hardware required for generating the test conditions may be untenable for many organizations. Herein, we discuss the development of the SVP testing capabilities for UL 1741 tests utilizing a controller hardware-in-the-loop (CHIL) testbed that precludes the need for power hardware using a 34.5 kW Austrian Institute of Technology (AIT) Smart Grid Controller (SGC). Analysis of normal ramp rate, soft start ramp rate, specified power factor, volt-var, and frequency-watt advanced grid functions and the effectiveness of the UL 1741 test protocols are included.

Index Terms — hardware-in-the-loop, CHIL, advanced inverter functions, UL 1741, certification testing.

I. INTRODUCTION

With the rapidly changing landscape of grid codes and interconnection standards [1-2], manufacturers of distributed energy resources (DER) components are under increasing pressure to reliably update and validate the interoperability and performance of their equipment for different regional requirements and grid conditions. In the U.S., the California Public Utilities Commission updated California Electric Rule 21 to include autonomous grid-support functionality in 2015 [3]. In response to the new requirements, Underwriters Laboratories (UL) published a revised UL 1741 [4] certification protocol with Supplement SA “Grid Support Utility Interactive Inverters and Converters” on September 7, 2016, that includes test sequences and pass/fail criteria for the new grid support functions. CA Rule 21 states that all DER equipment installed on Investor Owned Utility (IOU) systems shall be listed to UL 1741 one year after completion of the UL 1741 update: September 7, 2017. This has resulted in a recent surge of certification testing at the Nationally Recognized Testing Laboratories (NRTLs). The relatively short time to list products along with lengthy UL 1741 test times have caused vendor certification delays.

In a multi-year effort, Sandia National Laboratories and the SunSpec Alliance have been creating a versatile certification software platform that automates the UL 1741 test procedure by interacting with a range of test equipment. The open-source¹ SunSpec System Validation Platform (SVP) [5] enables research, vendor, and NRTL power laboratories to perform evaluations quickly and effectively. The SVP has been successfully deployed for interconnection and interoperability testing of DER devices [2, 5-7], demonstrations of DER voltage regulation [8] and characterization of DER for hardware-in-the-loop environments [9] previously. The primary goal of the SVP software is to provide complete certification and automatic evaluation of DER grid-support behavior. However, the requirements for full power system testing are formidable—especially for large power stages—making prototyping and firmware improvements difficult to implement in short timeframes.

In order to enable rapid prototyping of grid-tie inverter controllers, the Austrian Institute of Technology (AIT) and SNL have been collaborating under the auspices of the Smart Grid International Research Facility Network (SIRFN) Annex of the International Smart Grid Action Network (ISGAN) to develop a new approach for rapid and concurrent development of controls and application software [6]. The technique

¹ The collection of test logic (SVP scripts) and equipment drivers (SVP Energy Lab) is regularly updated on the SunSpec GitHub site: https://github.com/sunspec
expands on previous SIRFN power systems research on DER grid-support function evaluations [2, 7] by using a controller hardware-in-the-loop (CHIL) testbed integrated with the SVP automated testing platform. The CHIL-SVP research platform is expected to help equipment vendors meet evolving grid standards by systematically validating DER performance and system improvements during the design cycle. This methodology provides key benefits over traditional full-scale power laboratory testing by minimizing the power equipment required to evaluate the system while also evaluating control logic and interoperability interfaces prior to integration with hardware. The CHIL test setup also has the flexibility to operate for a range of systems, e.g. single and three-phase devices, different nameplate ratings, grid functions, and operating capabilities.

This paper describes this novel CHIL-SVP testing methodology for UL 1741 SA requirements and demonstrates the capacities of the AIT integrated SunSpec-compliant server and smart grid controller. The remainder of the paper is structured as follows: Section 2 describes the CHIL-SVP integrated test setup, Section 3 contains results from a subsection of the UL 1741 SA tests, Section 4 discusses the pros and cons of this approach and the UL 1741 SA test protocol, and Section 5 concludes the paper.

II. LABORATORY TESTBED CONFIGURATION

The UL 1741 certification tests were conducted on a CHIL system consisting of an advanced smart grid controller (SGC) connected to a real-time simulation system (Typhoon HIL 602). The HIL 602 unit provided a real-time \( \mu s \) resolution simulation of the converter power stage, the AC power grid and the solar array and connects to the SGC through analogue and digital inputs and outputs, representing grid voltages, currents, and IGBT PWM signals. The AIT SGC HIL Connect unit [10-12] and a commercial PC were also used in the experiments to control the automated test setup, as shown in Fig. 1.

The equipment under test (EUT) represents a two-quadrant 34.5 kW grid-tie PV inverter providing a broad range of advanced grid support capabilities. The EUT modes and settings—controlled by the SGC, in this case—are accessed through a dedicated communications processor running a SunSpec Modbus TCP server that handles the low-level communication with the SGC via a secured binary protocol. Fig. 2 shows the internal layout of the HIL Connect and the connectivity features. The DC power was provided by simulated PV array with maximum power point \( P_{mpp} = 36.24 \) kW at 1000 W/m².

The SVP was utilized as the central control platform to run the UL 1741 SA test protocols, as shown in Fig. 3. The SVP is designed such that:

1. All simulated and physical power system testing equipment are abstracted so the test logic is fixed for all laboratory environments. This enables portability of the test sequences.
2. SVP tests are designed to be modular so cases which cause failures or other unwanted behavior can be studied in closer detail.
3. Tests can be grouped into sequences of experiments so groups of test or the entire UL 1741 SA protocol can be run autonomously.
4. The test environment and EUT parameters are adjustable through a GUI interface. These parameters can be applied at the global level for all tests in a suite to minimize configuration time.

For the experiments in Section 3, the EUT settings were changed via SunSpec Modbus over TCP/IP, and the grid conditions (voltage, frequency), available DC power (PV simulator irradiance), and data measurement equipment were controlled with the Typhoon HIL Application Programming Interface (API).
III. EXPERIMENTAL RESULTS

The CHIL-SVP setup is capable of testing the EUT compliance to any number of grid codes and standards. Here, the UL 1741 SA tests shown in Table I were programmed into the SVP to evaluate the SGC compliance to these functions. For some of the functions, partial or no functionality was included in the equipment. In those cases, only the default behavior of the equipment could be evaluated such as ramp rate response, specified power factor, volt-var, and frequency-watt test results were collected for this assessment. As new capabilities are programmed into the SGC, these modes will be tested against the UL 1741 SVP test scripts and presented in a future publication.

<table>
<thead>
<tr>
<th>UL 1741 SA Test</th>
<th>EUT Capability</th>
</tr>
</thead>
<tbody>
<tr>
<td>Anti-islanding Protection</td>
<td>No</td>
</tr>
<tr>
<td>Low and High Voltage Ride-Through</td>
<td>Nonprogrammable</td>
</tr>
<tr>
<td>Low and High Frequency Ride-Through</td>
<td>Nonprogrammable</td>
</tr>
<tr>
<td>Normal Ramp Rate and Soft-Start Ramp Rate</td>
<td>No</td>
</tr>
<tr>
<td>Specified Power Factor</td>
<td>Yes</td>
</tr>
<tr>
<td>Volt/Var (Q/V) Mode</td>
<td>Yes</td>
</tr>
<tr>
<td>Frequency-Watt (Optional)</td>
<td>Yes</td>
</tr>
<tr>
<td>Volt-Watt (Optional)</td>
<td>No</td>
</tr>
</tbody>
</table>

A. Normal and Soft Start Ramp Rates

The SGC did not include programmable ramp rates, but UL 1741 normal ramp rate (RR) and soft start (SS) experiments were conducted for the default operating parameters of the EUT to demonstrate the SVP test script and pass/fail criteria. For the normal ramp rate test, the rated AC current of the EUT was brought to 5% of nameplate by reducing power of the simulated PV system. Then the power of the PV simulator was returned to rated power and the response of the EUT was recorded. This was repeated three times for the maximum, minimum, and average ramp rate. In this case all the experiments assumed a 100% \( I_{rated} \) ramp rate, where \( I_{rated} \) is the apparent current rating of the EUT.

Depending on the source requirements document, there are different pass/fail criteria for average or maximum RR requirements. In the case of average RR, the EUT is compliant if it maintains the target ramp rate plus or minus the manufacturer’s stated accuracy of ramp rates. The criteria used for the maximum ramp rate is more detailed. The instantaneous power cannot exceed 150% of the target ramp rate and the average ramp rate cannot exceed the target ramp rate. Additionally, the response of the EUT between 10% and 90% of rated current is binned into 20 time periods in which the binned power cannot exceed 125% of the straight-line ramp rate and consecutive bin currents also may not exceed 125% the target ramp rate.

Normal ramp rate results are presented in Fig. 4. The response of the EUT is initially quick, but then the current drops and the EUT ramps back to rated current. As shown in the binned data in Fig. 5, the EUT is not compliant with the 100%/sec RR function because the instantaneous current is greater than 150% of the target current ramp rate and binned data exceeds the 125% limit in the first time period.

To evaluate the soft start ramp rate function, Phase A voltage was set to 0 V for five seconds to cause the EUT to trip. Then the voltage on phase A was returned to EUT nominal values and the response of the EUT was measured, as shown in Fig. 6. The target soft start ramp rate was set to 100% \( I_{rated} \)/sec. The pass/fail criteria using the maximum SS formulation was used and the bins for the 10% to 90% of \( I_{rated} \) open loop response time were created, shown in Fig. 7. In this case, the EUT passed all the acceptance criteria except that two data points at the beginning of the evaluation window exceeded 150% of the ramp rate.

![Fig. 4. Ramp rate response increasing EUT available current from 5 to 100%.](image-url)
B. Specified Power Factor

The UL 1741 SA power factor test requires four power factor value settings at three power levels (i.e., 20%, 50%, 100% of nameplate), three times each. For each of the 36 tests, the power factor is initially set to unity and then changed to the target power factor. Since the EUT is a fully two-quadrant converter, the PF could be reduced to zero. However, for these experiments, \( PF_{\text{min}} \) was set to 0.20. The settings were changed in the EUT through the SunSpec interface and the power factor was measured after three times the settling time of the EUT—a total of 3 seconds. Time domain data was collected at 5 samples/sec. The results of the tests are shown in Fig. 8 in an active-reactive power (P-Q) plane. The black dashed lines indicate the target power factors, the red dashed lines indicate the \( PF_{\text{target}} \pm MSA_{PF} \) pass/fail levels, and the four colored markers represent the EUT output for each of the PF levels. The manufacturer specified accuracy of power factor, \( MSA_{PF} \), was designated to be 0.03 for these experiments, though it should be noted that at low power factors the PF deviation will be higher. The EUT accurately reached the PF target within the passing bounds in all but three tests at \( PF = -0.20 \). The passing region surrounding the unity PF value was used to determine if the EUT was initially set to unity PF prior to issuing the PF command.

C. Volt-VAr Mode

The Volt-VAr Mode (Q(V)) is an autonomous control model to provide distribution circuit voltage regulation. The Q(V) test sequence from UL 1741 was completed with the CHIL-SVP setup. The Q(V) test requires three curves be measured at 15 or more AC voltage points in an increasing and
decreasing direction three times at two DC power levels (20% and 100% of nameplate) and five times at another power level (66% of nameplate). This sequence is repeated for Active Power Priority and Reactive Power Priority Q(V) modes, if both are supported. In the case of the SGC, only the Reactive Power Priority mode was tested with a reactive power nameplate capacity of 34.5 kVar. This test requires a large number of test permutations and measurements (990 or more for each mode) and would difficult without automation. The results for the three volt-var curves are shown in Figs. 9-11. The passing region is described by the target curve plus or minus manufacturer’s specified accuracy of reactive power \( \text{MSA}_{Q(V)} \), which was selected to be 2000 VA (5.8% nameplate reactive power) for these experiments.

As shown in all the curves, the EUT slightly mismeasured the grid voltage, which resulted in a shift of the reactive power points to the right of the programmed curve. This error pushed some of the reactive power points outside of the passing region in Curves 1 and 2. The EUT passes the Q(V) test for Curve 3 with the given \( \text{MSA}_{Q(V)} \). The two points above the -100% reactive power level in Curve 1 are because the EUT was not capable of providing 0 PF in this mode. Updating the reactive power nameplate capacity of the EUT for this mode would correct this offset.

### D. Frequency-Watt

The frequency-watt function is designed to support bulk system operation in the case of generation or load tripping. The function is typically programmed to only reduce power in overfrequency scenarios for PV systems (not increase output during underfrequency events) in order to maximize power production; although there is a growing set of research which shows the benefit of bidirectional FW functions for high-penetration solar scenarios [13, 14]. UL 1741 SA only accounts for the overfrequency case and specifically requires three or more frequency points to be measured above \( f_{\text{start}} \) (50.1 Hz here). However, it was difficult to distinguish the FW curve and evaluate the function from only three points, so 10 points were measured for these experiments. The frequency was swept up and down three times for three power levels (100%, 66% and 33% of \( P_{\text{rated}} \)) for two FW curves. After changing the grid frequency and waiting the EUT settling time \( t_s \), the pass/fail criteria was evaluated for a period of at least \( t_s \). During this time, shown in blue in Fig. 12, the EUT must be within the manufacturer’s stated FW accuracy of the FW curve, shown by the red curves. A single measurement from the end of the evaluation period was plotted in Figs. 13 and 14 to summarize the FW behavior of the EUT. Except in cases where the EUT was maximum power point tracking, the EUT was within the passing FW power levels.
IV DISCUSSION

The CHIL-SVP evaluation platform successfully executed four grid-support function certification tests using the AIT SGC as the EUT. The results showed the effectiveness of using the CHIL approach to assist programmers in designing DER firmware to catch design mistakes prior to deployment in hardware. The setup and operation of this type of testbed was significantly quicker and less expensive than running the experiments with power equipment and was easily deployed in an office environment.

The results also demonstrated the capabilities of the SGC to perform multiple grid-support functions. Tight manufacturer’s specified accuracies caused some of the advanced grid functions to not meet the UL 1741 SA criteria, but the capabilities of the specified power factor, volt-var, and frequency-watt function were well demonstrated through these experiments. The SGC did not include normal ramp rate or soft start ramp rate functionality, but the UL 1741 tests were conducted to demonstrate the test procedure. This and other grid-support functions will be evaluated using the full suite of UL 1741 SA test procedures in the future.

UL 1741 SA is anticipated to be updated in the next two years to include the functions prescribed in the IEEE 1547 revision. The new testing requirements will once again require vendors to initiate quick design cycle times; the CHIL-SVP testbed could help controller designers test firmware designs to UL requirements before hardware implementation, giving them confidence the integrated system will pass the certification tests without extensive redesign. The UL 1741 SA revision will also give the UL standards technical panel (STP) an opportunity to update and improve the current version of the standard. The following sections include recommendations to improve the effectiveness of the protocol.

A. Comments on UL 1741 RR and SS Tests

The normal ramp rate and soft start ramp rate test sequences effectively demonstrate the capabilities of the EUT to adjust the active power response. The number of tests and ramp rate range is sufficient to demonstrate and certify products. The pass/fail criteria for this test, however, is overly prescribed and complicated in the case of maximum ramp rate. Binning the response of the EUT between 10% and 90% of I rated requires extensive post-processing and does not appear necessary. Instead, it is recommended that pass/fail criteria be rewritten to state, “the EUT response shall not exceed the programmed ramp rate plus the manufacturer’s stated ramp rate accuracy.”

B. Comments on UL 1741 SPF Tests

The specified power factor test sequence in UL 1741 SA balances the number of tests with assessment sufficiency well. The principal challenge of the test is that, if the EUT has a wide range of PF settings, using the MSA Pf is not effective at low PF values because the passing envelope becomes small. This could be improved by assessing the performance using a

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Fig. 12. Frequency domain results for one sweep of Curve 2 at 100% DC Power.

Fig. 13. EUT FW response for Curve 1.

Fig. 14. EUT FW response for Curve 2.
manufacturer’s stated accuracy of phase angle, MSA_{Ph}, as opposed to MSA_{PF}.

C. Comments on UL 1741 Q(V) Tests

The Q(V) test requires nearly a thousand reactive power measurements for Active Power Priority or Reactive Power Priority modes. Using a 2 second settling time, testing one mode required 1 hour and 35 minutes. While this may seem excessive, it does accurately characterize the behavior of the EUT. If automated scripts are used, it is not necessary to reduce the number of permutations for this test. However, if desired, the number of tests could be reduced by eliminating some measurement repetition (especially the five repetitions required at 66% power) or the requirements to assess Q(V) hysteresis.

The acceptance criteria for the volt-var function states, “the EUT reactive power measurement should remain within the manufacturer’s stated accuracy of the Q(V),” where the MSA_{Q(V)} is given by the reactive power accuracy. This criterion does not account for equipment with high reactive power accuracy but low voltage measurement accuracy. In the case of the SGC, the MSA_{V} is estimated to be ±1%. Taking this into account, the pass/fail band should be re-drawn to that in Fig. 10 and the EUT would pass the test. It is believed not accounting for MSA_{V} in UL 1741 SA Q(V) tests is an oversight.

![Volt-Var Function 2](image)

Fig. 15. Q(V) pass/fail criteria accounting for the EUT voltage accuracy.

D. Comments on UL 1741 FW Tests

In comparison to the volt-var tests in UL 1741 SA, the frequency-watt test sequence does not characterize the curve of the EUT in sufficient detail. Requiring only three frequency measurements to be taken above f_{syst} does not sufficiently demonstrate system behavior, although individual NRTLs may choose to sample the FW response at more frequencies. Instead, it is recommended that active power of the EUT is measured every 0.1 Hz between the minimum and maximum frequencies of the widest programmable near nominal frequency ride-through region of the EUT. This would not require more time than the volt-var test and it would fully characterize the FW behavior of the EUT. As an example, higher FW sampling rate results are provided in [9].

Additionally, the FW acceptance criteria should be clarified. First, it is not possible to fall within the commanded active power characteristic when the input power is at 33% and 66% so it is assumed that the passing region must be re-drawn as shown in Figs. 13 and 14—with the dashed lines—to represent the available EUT power. Furthermore, the acceptance boundary is ambiguously defined based on an offset relationship using MSA_{P0} and MSA_{Hs}.

V Conclusions

SNL, AIT, SunSpec Alliance, and Typhoon HIL are collaborating to create an automated SVP evaluation platform. The effectiveness of this approach was demonstrated for four grid-support functions, along with recommendations for the UL 1741 SA test protocols based on experiences implementing the procedure. When coupling the SVP with a CHIL testing environment, the integrated testbed and associated capabilities enabled users to:

1. Complete certification experiments with limited power system hardware, e.g., grid simulator, PV simulator, data acquisition system, RLC loads, etc.
2. Test large EUT controllers prior to integration with high-power equipment.
3. Accelerate the design cycle for DER interconnection and interoperability compliance.

Sandia and SunSpec are releasing SVP scripts—including the UL 1741 SA tests—in an online repository for DER vendors, NRTLs, and researchers to use, evaluate, and improve. It is the intention of the team to provide a standardized testing sequence, evaluation logic, and report generation for all interested parties. Ultimately, this has the potential to accelerate interconnection and interoperability testing and standardize the certification process across the solar industry.

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