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Communication Signal for Rapid Shutdown Test Specification



Abstract

This document defines the test requirements and procedure for conducting electrical tests to verify compliance with the *SunSpec Interoperability Specification: Communication Signal for Rapid Shutdown*.

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2	01-04-2017	in Section 2.2.1
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SunSpec interoperability specifications follow this lifecycle pattern of DRAFT, TEST, APPROVED and SUPERSEDED.

For more information or to download a SunSpec Alliance specification, go to <u>http://sunspec.org/about-sunspec-specifications/</u>.

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References:

[1] "Communication Signal for Rapid Shutdown: SunSpec Interoperability Specification"

1. Introduction

The purpose of this document is to define a test procedure to check the compliance of equipment with the SunSpec Communication Signal for Rapid Shutdown specification. Checking the compliance of equipment is done in two steps:

- The equipment will be first tested according to the electrical specification defined by SunSpec either as a transmitter or a receiver
- A second functional test of inter-operability between equipment from various suppliers can then be performed

Section 2 of this document covers the transmitter electrical test

Section 3 of this document covers the receiver electrical test

Section 4 of this document defines the interoperability test process

Section 5 of this document defines the interoperability test sequences

Operating temperature conditions: electrical parameters shall be checked at temperatures specified by the manufacturer.

2. Transmitter electrical test specification

2.1. Principle of transmitter electrical test

This part of the test specification refers to paragraphs 6.1 and 6.3 of the document "Communication Signal for Rapid Shutdown: SunSpec Interoperability Specification" [1]

The purposes of the test of the transmitter are the following:

- Test the modulation accuracy of the transmitter according to table 6 of paragraph 6.3 of [1]
- Test the output level and impedance of the transmitter according to table 6 of paragraph 6.3 of [1]
- Test the output spectrum of the transmitter according to paragraph 6.1 of [1]

Figure 2.1 gives a generic test environment for the test of the transmitter:

- DUT is the transmitter device that has to be tested
- Enabling equipment is the equipment necessary to put the transmitter in operation but not influencing the key electrical parameters of the transmitter (it could be external power supplies for the transmitter, equipment to simulate the voltage of a PV string if the transmitter is part of an inverter, ...)
- Test equipment is the equipment that will be used to extract the electrical parameter that has to be tested.
- Load is a reference component on which the transmitter delivers its signal and on which the test equipment extracts the electrical parameter that has to be checked.



Figure 2.1 transmitter test configuration

2.2. Transmitter electrical performance test

2.2.1.Modulation accuracy test

The reference for this test is table 6 of paragraph 6.3 of [1]

Test of the frequency accuracy: the test is performed according to figure 2.2.



Figure 2.2: test of frequency accuracy

For the test of the frequency accuracy, we propose a test mode to be implemented in the product embedding the transmitter device in order to send a permanent signal at FM or FS. In this mode, the transmitter is connected to a one (1) Ohm load resistor. The frequency counter checks the accuracy of FM and FS frequencies of the keep alive signal on the load resistor according to table 2.1.

Symbol		Min.	Тур.	Max	Unit
FM	Mark Frequency	131.236875	131.25	131.263125	kHz
FS	Space Frequency	143.735625	143.75	143.764375	kHz

Table 2.1: frequency accuracy

Test of the signal timing and waveform accuracy: the test is performed according to figure 2.3.



Figure 2.3 test of signal timing accuracy

The post-processing steps from the captured data shall comprise the following operations:

- 1. Demodulation of the FSK data to a baseband NRZ signal proportional to the transmitted bit values at the same sample rate as the original capture. This NRZ signal should be truncated to an integer number of duty-cycle periods at the desired sample rate, *e.g.*, 9 whole duty cycles.
- Performing a circular, normalized cross-correlation of the NRZ demodulated waveform from step #1, with an ideal waveform template consisting of the sequence {W1,W1,W1} that has been zero-padded to the same length as the demodulated NRZ signal.
- 3. Searching for all correlation peaks with a correlation coefficient of >0.9, and verifying their peak locations and magnitudes.

Mathematical Detail:

Demodulation of the captured waveform shall be accomplished by subtracting the magnitude of the output of a matched filter at the mark-tone frequency from the magnitude a matched filter at the space-tone frequency, where both matched filters take their inputs from the entire vector of captured data. This may be written as:

$$d_{k} = \left| \sum_{i=0}^{N} M_{-}b_{k} \cdot x_{n-i} \right| - \left| \sum_{i=0}^{N} S_{-}b_{k} \cdot x_{n-i} \right|,$$

where $\{M_b_k\}$ are the complex coefficients of the mark-tone matched filter, and $\{S_b_k\}$ are the complex coefficients of the space-tone matched filter and $\{x_i\}$ are discrete samples of the captured waveform.

The samples of $\{d_k\}$ shall be truncated to a length of nine duty cycle periods, such that its length is $N = 9 \times 11 \times 19 \times F_s \times T_b$ samples, where F_s is the sample rate and T_b is the bit duration. Let the resultant vector be notated as d.

Let the ideal waveform template representing the sequence {W1,W1,W1}, be notated as a vector w, having $M = 11 \times 3 \times F_s \times T_b$ non-zero samples, but padded with zeros to length N. Further, let the periodic summation of w with a period of N be notated as w_N .

The required circular correlation can now be written as:

$$\boldsymbol{r} = \sqrt{L} \cdot \frac{(\boldsymbol{d} \star \boldsymbol{w}_N)}{\|\boldsymbol{d}\| \times \|\boldsymbol{w}\|} ,$$

where *L* is the number of duty cycle periods (*i.e.*, the expected number of correlation peaks), \star is the correlation operator and $\|\cdot\|$ represents the norm of its vector argument. The resultant vector *r* has *N* samples, the same length as vector *d*.

Based on the convolution theorem, the equivalent result can be obtained as follows:

$$\boldsymbol{r} = \frac{\sqrt{L}}{\|\boldsymbol{d}\| \times \|\boldsymbol{w}\|} \left(\mathcal{F}^{-1} \{ \mathcal{F} \{ \boldsymbol{d} \} \cdot (\mathcal{F} \{ \boldsymbol{w} \})^* \} \right).$$

Where $(\cdot)^*$ means complex conjugation, $\mathcal{F}{x}$ is the Fourier transform of the vector x, and $\mathcal{F}^{-1}{X}$ the inverse Fourier transform and $X \cdot Y$ represents element-wise multiplication of two vectors.

The following limits shall be verified:

- 1. The timing interval errors (TIEs) assessed by the locations of at least 8 correlation peaks relative to the first detected correlation peak shall not exceed ±100ppm of the respective measured time intervals.
- 2. The correct number of correlation peaks shall be detected for a given data set size given by the number of whole duty-cycle periods included in the capture. (Nine peaks are expected.)
- 3. The correlation coefficient for each detected peak shall exceed 0.99 (99%).

2.2.2.Transmitter output level test and transmitter output impedance:

The reference for this test is table 6 of paragraph 6.3 of [1]

- This test is performed according to figure 2.4 by varying the load resistor on the DUT and checking the signal level at frequency FM and FS on the spectrum analyzer according to table 2.3.
- To check the transmitter maximum output dynamic, the load resistor is set to 100kOhms.
- To check the output impedance the load resistor is set to 1 Ohm and the min and max output level measured on the spectrum analyzer assumes that the output impedance of the DUT varies between 0.05 Ohms and 1.5 Ohms.



Figure 2.4: transmitter output level test

Symbol		Min.	Тур.	Max	Unit	Comment
VTX	high load output swing	0.9	1	1.1	Vrms	Rload=100kOhms
Viend	tuo na mittan ao malia na a	0.20		1.05)//////////////////////////////////////	Rload=10hms> calculate
vioad	transmitter compilance	0.36		1.05	VIIIIS	transmitter output impedance

Table 2.3: Transmitter output level and output impedance test

2.2.3.Transmitter in band spurious emission test

The reference for this test is paragraph 6.1.10 of [1]

The tested transmitter is put in test mode as proposed in part 2.2.1 and configured to generate a single frequency signal at FM or FS. The test is performed according to figure 2.6, and the measured sprectrum on the

output of the DUT should fulfill the mask defined at figure 2.5. The two mark and space signals at FM and FS are taken as the reference level (0dBc) in the spectrum mask of figure 2.5.



Figure 2.5: transmitter in band spurious emission mask



Figure 2.6 Schematic for in band and out of band test

For in band emission test, the following configuration should be used:

- The mark or space frequency are sent separately (a test mode needs to be implemented as defined in the compliance test specification)
- Rload is set to 10 Ohms
- Spectrum analyzer attenuation : 40dB (20+20)
- Frequency span : centered on the PLC frequencies, frequency span 60kHz or more
- Detection method : positive peak detector
- Resolution bandwidth : 30Hz or less

2.2.4. Transmitter out of band spurious emission test

The reference for this test is paragraph 6.1.9 of [1]

The test is performed according to figure 2.6 and the measured spectrum on the output of the DUT should fulfill the mask defined at figure 2.7. In order to measure only the contribution of the transmitter to the out of band spectrum, the PV inverter could be switched off during this test.



Figure 2.7: transmitter out of band spurious emission mask

For out of band emission test the following test configuration should be used:

- The PLC signal is sent continuously (in test mode, W1 is sent continuously)
- Rload is set to 10 Ohms
- Spectrum analyzer attenuation : 40dB
- Detection method : positive peak detector
- Start frequency: 50kHz or less
- Stop frequency: 500kHz or more
- Resolution bandwidth : 30Hz or less
- Video bandwidth : 10Hz or less

3. Receiver electrical test specification

3.1. Principle of receiver test

This part of the test specification refers to paragraphs 6.2 and 6.3 of the document "Communication Signal for Rapid Shutdown: SunSpec Interoperability Specification" [1]

The purposes of the test of the receiver are the following:

- Test the sensitivity level and the maximum input signal level acceptable on the receiver to *indicate the presence* of a permission to operate signal according to requirement 6.2.2 and to table 6 of paragraph 6.3 of [1]
- Test the capability of the receiver to *indicate the absence* of a keep alive signal in presence of a signal compliant with any other SunSpec compliant code other than the permission to operate signal according to requirement 6.2.4 and to table 6 of paragraph 6.3 of [1]
- Test the capability of the receiver to *indicate the presence* of a permission to operate signal according to requirement 6.2.2 and to table 6 of paragraph 6.3 of [1] in presence of both in-band and out of band interferers as defined in part 6.2.6 and 6.2.7 of [1]
- Test the capability of the receiver to *indicate the absence* of a permission to operate signal according to requirement 6.2.2 and to table 6 of paragraph 6.3 of [1] in presence of both in-band and out of band interferers as defined in part 6.2.6 and 6.2.7 of [1]

Informative note:

For in-band and out-of-band interference tests, the major point to be tested is the de-sensitization of the receiver due to blocking interferers. It is also considered that intermodulation products have less impact than blocking signals on the performance of the receiver. The interferer rejection test is done through single tone interferers coupled at the input of the receiver. In that way it is possible to validate in a single test the linearity of the receiver and the performance of the digital demodulator in the presence of interfering signals.

Figure 3.1 gives a generic test environment for the test of the receiver:

- DUT is the receiver device that has to be tested
- Enabling equipment is the equipment necessary to put the receiver in operation but not influencing its key communication electrical parameters (it could be external power supplies, equipment to simulate the voltage of a PV module if the receiver is attached or embedded in a PV module, ...)
 - SunSpec signal pattern generator is an equipment able to generate a signal compliant with table 6
 of paragraph 6.3 of [1] both for the permission to operate signal, but also other codes defined in 6
 (accelerated shutdown,...). This reference signal generator should be able to deliver powerful
 enough signals in order to test the receiver at maximum output voltage. This signal generator could
 be a suitably buffered arbitrary waveform generator configured to operate at a sample rate of at

least 400kHz and having a memory depth sufficient to store an entire SunSpec duty cycle period of 1.07008 seconds. It could also be a "golden reference" transmitter being made of a transmitter device compliant with the electrical specification defined in part 2. No matter how it is constructed, the SunSpec signal pattern generator must be verified to pass the Transmitter electrical performance tests specified in section 2.2 of this document.

- Single tone generator is a programmable signal generator to test both in-band and out-of-band spurious rejection of the receiver.
- Indicator is the way the receiver indicates that he has decoded or not a permission to operate signal as defined in requirements 6.2.2 and 6.2.4 of [1]



Figure 3.1 Receiver test configuration

3.2. Receiver electrical performance tests

3.2.1.Receiver input range electrical test:

The references for this test are paragraphs 6.2 and 6.3 of [1].

The purpose of this test is to check the sensitivity level and the maximum input signal level acceptable on the receiver to *indicate the presence* of a permission to operate signal. It is also to test the capability of the receiver to *indicate the absence* of a keep alive signal in presence of a signal compliant with any SunSpec compliant code other than the permission to operate pattern.

The test is performed according to figure 3.2. The signal level at FS and FM is measured at the input of the DUT according to the levels defines in table 3.1. The result of the test is validated through the permission indicator output according to table 3.1 ("permission indicator" column).



Figure 3.2: Receiver input range electrical test diagram

Test signal pattern	FS, FM signal level	Permission indicator
A,B,C,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z with ABC=W1,W1,W1	1.2mVRMS or -58.4dBVrms	YES
A,B,C,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z with ABC=W1,W1,W1	142mVRMS or -17dBVrms	YES
A,B,C,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z with ABC= all other Suspec combinations except W1,W1,W1 ; W0W1W0 ; W1W1W0 and W0W0W1	1.2mVRMS or -58.4dBVrms	NO
A,B,C,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z,Z	142mVRMS or -17dBVrms	NO

Table 3.1: Receiver input range test conditions

3.2.2.Receiver in band interferer rejection

The test is performed according to figure 3.3. The interfering signal is a CW tone sent with a varying frequency between 120kHz and 155kHz according to table 3.2 and Figure 3.4.

CW freq. (KHz)	120	122.5	123.75	125	126.25	127.5	128.75	130	131.25	132.5	133.75	135	136.25	137.5
CW level (mV)	17	17	17	17	17	17	1.7	1.7	1.7	1.7	1.7	17	17	17
CW freq. (KHz)	138.75	140	141.25	142.5	143.75	145	146.25	147.5	148.75	150	151.25	152.5	155	
CW level (mV)	17	17	1.7	1.7	1.7	1.7	1.7	17	17	17	17	17	17	

Table 3.2: CW interferer frequency and signal level

It has to be noted that CW blockers at FM and FS are included in this test. The goal is to test that the architecture of the receiver is immune to any single tone blocking signal right at FS or FM.

As defined in the test specification two tests will be performed to test the in-band interferer rejection of the receiver:

Test1: the level of the SunSpec test pattern is measured at the input of the DUT at FS and FM and this level is set at "sensitivity level" +3dB i.e. 1.7mVrms or -55.4dBVrms. The test should begin with the "permission to operate signal already enabled from the SunSpec test pattern generator. The receiver should always indicate

the presence of a "permission to operate" signal after a dwell time of maximum 13 seconds for the each blocking frequency. This test should begin with the "permission to operate" signal already enabled from the SunSpec test pattern generator.

Test2: the SunSpec test pattern generator does not generate any signal. The in-band interferer signal generated by the tone generator is measured at the input of the DUT and both the frequency and the signal level are adjusted to the levels defined in Table 1. When sweeping the interferer level and frequency over the specified range of table 1, *the receiver should always indicate the absence of a "permission to operate" signal* after a dwell time of maximum 13 seconds.







Figure 3.4: test conditions for in-band interferer test.

3.2.3. Receiver out of band interferer rejection:

The test will be performed according to figure 3.3

The test of out of band interferer rejection is similar to the test of in band interference rejection but with CW blockers frequency and level corresponding to Table 3.3 and Figure 3.5. Two tests similar to the tests for inband interference are performed for each blocker CW frequency. The test should begin with the "permission to operate signal already enabled from the SunSpec test pattern generator.

CW freq. (KHz)	10	20	30	40	50	60	70	80	90	100	110	160	170	180
CW level (mV)	540	540	540	170	170	170	170	17	17	17	17	17	17	17
CW freq. (KHz)	190	200	250	300	400	500	600	700	800	900	1000			
CW level (mV)	17	54	54	54	170	170	170	170	170	170	170			

Table 3.3: CW interferer frequency and signal level

- Test 1: the purpose of this test is to check the capability of the receiver to *indicate the presence* of a permission to operate signal in presence of an out-of-band interferer as defined in figure 3 part 6.2 of [1].
- Test 2: the purpose of this test is to check the capability of the receiver to *indicate the absence* of a permission to operate signal in presence of an out-of-band interferer as defined in figure 3 part 6.2 of [1].

For test1, the level of the SunSpec test pattern is measured at the input of the DUT at FS and FM and this level is set at "sensitivity level" +3dB i.e. 1.7mVrms or -55.4dBVrms. The out-of-band interferer signal generated by the tone generator is measured at the input of the DUT and both the frequency and the signal level are adjusted to the levels defined in figure 3.5. When sweeping the interferer level and frequency over the specified range, the receiver should always indicate the presence of a "permission to operate" signal. The test should begin with the "permission to operate" signal already enabled from the SunSpec test pattern generator.

For test2, *the SunSpec test pattern generator does not generate any signal*. The out-of-band interferer signal generated by the tone generator is measured at the input of the DUT and both the frequency and the signal level are adjusted to the levels defined in Figure 3.5. When sweeping the interferer level and frequency over the specified range, *the receiver should always indicate the absence of a "permission to operate" signal*.





3.2.4. Receiver impedance test:

The reference for this test is paragraph 5.3 of [1] and Footnote 5 of Table 6.

The test will be performed according to Figure 3.1. The goal of this test is to check that the impedance of the receiver is within the limits defined in Table 6 of [1] (i.e. 0.7 to 1.5 Ohm).

A single tone generator is sending a signal at FM=131.25 kHz and in a furthermore test at FS=143.75 kHz across a 1:1 signal transformer to the DC output of the receiver-device under test. The signal voltage level shall

be once adjusted and then hold to reach measured ac-voltages in the range of up to 120 mV. A non-inductive shunt resistor is placed between the single tone generator and the DUT with the value of 1 Ohm and with 0.1 % tolerance. Furthermore a current source is placed in series to this tests circuit, to be able to inject a DC bypass current (current direction equal to normal operation mode).

The relation of the ac-signal magnitude measured directly at the DC output of the receiver-device at FS and FM divided by the level of the ac-signal measured at the shunt resistor shall be within the limits defined at Table 3.2. The ac-signal magnitude measuring at the receiver-device has to be performed directly at the DC output without the module wiring or any other additional wiring between point of measuring and the DC output of the receiver-device, considering Footnote 5 of Table 6 of [1]. The tolerances of ac-signal voltage measurements shall be less than 0.5%. The measured ac-voltages with an active current source and an inactive tone generator shall be less than 1.0 mV (optionally use additional filter to suppress harmonics of the current source). The test shall be performed with zero dc current and with the maximum rated dc current specified by the manufacturer of the DUT. This test shall be performed with at least 10 different DUTs.



Figure 3.6: Receiver impedance test setup

Symbol	Test conditions	Min	Max
	Generator output is set to FM=131.25 kHz		
U2/U1	and FS=143.75 kHz; signal voltage is	0.7	1.5
	adjust and hold to achieve measured	0.1	
	voltages up to 120 mV; Bypass-current is		

set to zero and maximum rating of DUT; U2 is measured directly at the dc output of the DUT, U1 is measured at a 1 Ohm, 0.1% shunt resistor

Table 3.4: Receiver input impedance test conditions

3.2.5. Receiver shutdown output voltage test

This test is suitable for a unit consisting of a receiver and associated switches to control the power of a PV module. In a typical application this unit will be integrated into the junction box of a PV module. This unit has one or more input ports for a serial connection of PV cells and one switched output port, where the PV voltage is available in case the enabling signal is present.

The tests are conducted with no enabling signal present. The unit is in shutdown mode.

Aim of the test is to check the conformance of the unit to the requirements on I_{OFF} and I_{OFFHI} in Table 1 "Mode Transition Parameters" in section 4.5 of the standard *(include suitable reference)*.

The test can be performed by supplying power to the device under test from either a PV module or a DC sources. Therefore two test setups are specified, but just the suitable one shall be performed.

3.2.6.Test setup 1 – powered by PV module

The unit is tested when mounted into the junction box of a PV module and connected to the cell strings of the module in a way specified by the manufacturer. The module has to be illuminated with enough light to conduct the tests. The irradiation has to be stable during the measurement. At the output port a variable load is connected.

3.2.7.Test setup 2 – powered with DC sources

The unit is powered by one or more DC power sources connected to its input ports. The setting of these power supplies has to be chosen in a way that the test are not influenced by the lack of DC power and the maximum ratings of the units are not exceeded. The voltage of the DC power supply has to be stable during the measurement. At the output port a variable load is connected.



3.2.8.Test procedure

The variable load is decreased until an output current of 10 mA is reached. At 10 mA the unit has to be operated for a minimum time of 1 Minute. During this procedure (ramp up and operation at 10 mA) the output voltage is measured. If the output voltage equals or exceeds 0.6 V with an output current from 0 mA to 10 mA the criteria for I_{OFF} has been met. Current and voltage have to be recorded for the measurement report.

If the unit includes the option "high power" for the shutdown mode the test has to be executed with an output current of up to 400 mA instead of up to 10 mA. If the continuous output voltage equals or exceeds 0.6 V with an output current of up to 400 mA the criteria for I_{OFFHI} has been met. Current and voltage have to be recorded for the measurement report.

3.2.9.Measurement equipment

Current and voltage will be measured with a maximum error of 1% of the measured value.

4. Equipment interoperability test specification

4.1. Technical Interoperability definition

For telecommunication standards, **Technical Interoperability** is usually associated with hardware/software components, systems or platforms that enable machine-to-machine communication to take place. This document covers the **Technical Interoperability** of equipment embedding Rapid shutdown communication signal transmitters and receivers from two different manufacturers.

The Technical Interoperability of telecom equipment is generally performed during Plugtest events where transmitters and receivers from various manufacturers are connected together and specified interoperability tests (such as defined in part 2 of this document) are performed. At the end of the Plugtest events, tests are documented (as defined for each test of part 2) and a compatibility list of equipment could be created as proposed in table 4.1.

Transmitter	Receiver
Manufacturer A	Manufacturer B
Equipment reference A1	Equipment reference B1
	Equipment reference B2
	Equipment reference Bn
Equipment reference A2	Equipment reference B1
	Equipment reference B2
	Equipment reference Bn

Table 4.1: example of a list of interoperable equipment compatible with the SunSpec Rapid Shutdown specification

The following interoperability test does not cover all possible circumstances. Thus a passed interoperability test will not guarantee full interoperability or a proper function.

4.2. The prerequisite to interoperability test:

To perform the interoperability between a transmitter and a receiver, it is assumed that both devices have fulfilled the electrical conformance test for the Rapid Shutdown Communication Signal.

4.3. Symptoms of interoperability and non-interoperability:

Symptoms of interoperability:

From a Rapid Shutdown standpoint, two devices from two different manufacturers are considered as interoperable if based on an action from the transmitter, the proper behavior is shown by the receiver. The proper behavior corresponds to electrical and timing specifications as listed in [1].

In part 5 of this document, the different inter-operability tests, scenarios, and the expected actions of both the transmitter and receiver are defined.

A proper interoperability test of two different devices could be defined in the following manner:

• "Start process" test:

When the initiator is set in a permission to operate position, the transmitter sends a keep alive signal on the DC power line, the receiver demodulates the signal and connects the PV module on the string. This test is performed in conditions corresponding to short and long PV strings

• - "Stop process" test:

When the initiator is switched to the Rapid Shutdown position, the transmitter stops sending the keep alive signal on the DC power line, the receiver detects that the signal is stopped and the output of the receiver to the PV string is set in standby mode according to the timing and electrical specification defined in [1]. This test is performed in conditions corresponding to short and long PV strings.

• "Repeatability and robustness of the interoperability" test:

The criticality of interoperability test is that the Rapid Shutdown function is targeted to be a safety feature of the PV installation, involving equipment from different manufacturers for the transmitter and the receiver.

The robustness (FMEA) and Safety Integrity Level of both the transmitter and receiver are supposed to be handled by both manufacturers during the design of their products. However, the repeatability of the interoperability of the emitter with the receiver should be checked through a minimum number of start and stop processes. Arbitrarily, we propose to do 5 cycles of "start and stop" tests during the Plugtest considering that a regular verification (e.g. yearly) of the rapid shutdown functioning will have to be recommended, e.g. during the maintenance of the PV installation.

• "Multiple receivers' interoperability" test:

In [1], it is defined that a single transmitter could be connected to up to 10 strings with up to 30 PV modules each. Interoperability test of 300 receivers with 1 transmitter does not look realistic in a plugtest. In part 5.4, we propose a test of 3 parallel receivers with a varying serial impedance simulating different length of strings.

Symptoms of non-interoperability:

There are two symptoms of non-interoperability:

- The receiver does not start or re-start properly after receiving a keep alive signal from the transmitter. This could be due to several reasons: the level/timing of signal received from the transmitter (long strings, multiple strings), the receiver demodulator performance, and the locked-in of the receiver due to some transient behavior.
- The receiver does not perform the rapid shutdown properly and according to the reference specification [1].

One of the goals of the plugtest is to ensure that instances of non-interoperability are not caused by poor or insufficient definition of the interoperability tests. For this purpose, and in order to find the root causes of non-interoperability, we propose to constantly monitor the DC line at the input of the receiver as defined in the overall interoperability test framework of part 4.4.

4.4. Overall interoperability test framework:

Figure 4.1 shows the principle schematic for testing the interoperability of a transmitter from manufacturer A with a receiver from manufacturer B:

- To reduce the complexity of the test and the test time, we propose for the 3 first tests defined in part 1.3 to use one single receiver associated with one transmitter.
- To evaluate the impact of the number of modules per string and the length of the string wires, a varying line impedance ZL shall be inserted on the string. Impact of parallel strings could also be simulated by inserting a parallel impedance at the output of the transmitter if needed.
 One pv module with an added receiver has to be simulated by an inductance of 2.2µH to 2.9µH (including tolerances). This value simulates the impedance of one receiver together with the impedance of the wiring of one pv module.

The additional wiring per string has to be simulated with an inductance from 0 μ H up to the value of 220 μ H for the longest string.

• To evaluate the impact of parallel strings a parallel impedance at the output of the transmitter shall be inserted.

One pv-module with an added receiver has to be simulated by an impedance of 1.8 Ohm to 2.6 Ohm (including tolerances). This value simulates the impedance of one receiver, together with the impedance of the wiring of one pv module.

For the additional parallel strings we consider that a total of 10 strings are connected in parallel with a wire length for each string corresponding to long wires.

- If the receiver is integrated inside a PV module, means will have to be provided to give power to the receiver. Otherwise, for receivers embedded inside a retrofit box, the PV modules could be simulated by a DC power supply connected to the receiver.
- If the transmitter is embedded in an inverter, and if the inverter needs a minimum string voltage to
 operate properly, a serial controlled voltage source could be inserted in the string to reach this
 minimum operating voltage. If the output impedance of this voltage source at the communication
 frequencies is not negligible, a suitable capacitor has added to the output of the controlled voltage
 source.
- If the transmitter needs the right standby voltage to start up, an additional controlled voltage source could be inserted in series. At this point it is possible to use a low power supply or a current restricted supply, if this voltage source is bridged by a bypass diode. If the output impedance of this voltage source at the communication frequencies is not negligible, a suitable capacitor has added to the output of the controlled voltage source.

• String voltage and string current are monitored at the output of the receiver to validate the rapid shutdown operation and the start behavior on their 3 key parameters: string current, string voltage and timing.

Depending on manufacturers of transmitters and receivers, the installation manuals and product data sheets could use different numbers of panels in series and strings in parallel for worst case testing. In this case, the interoperability test framework could be adapted to the limits defined by the manufacturers, stating in the interoperability table (table 4.1) the specific limits considered in the interoperability test.



Figure 4.1: Principle of interoperability test framework

5. Interoperability test sequences

5.1. Start Process interoperability test: single receiver

The "start process" interoperability test is performed according the principle schematic shown in figure 4.1.

The test process is described in table 5.1 and the timing diagram is shown in figure 5.1.

Interoperability test description							
Identifier	"Start process" from a Rapid shutdown position						
Test objective	Verify that when the transmitter starts from a rapid shutdown position of the initiator, the transmitter sends the keep alive signal properly, the receiver properly demodulates the signal and activates the control of the PV module. This test shall be performed with a) a single long (ZL=284 to 304μ H + DUT) and b) a single short string (ZL=11 to 14.5μ H + DUT) and c) a single short string with a long string wiring (ZL=11 to 14.5μ H + 220 μ H + DUT) and Zp corresponding to 9 parallel strings of 6 modules with an average short string wiring impedance (Zp=10 Ohm equal to 90 Ohm per string, each with max. 10% tolerance)						
Pre-test conditions	The initiator is in rapid shutdown position, the transmitter and the receiver are properly powered (the receiver is connected to a PV module with sun or is connected to a DC supply simulating a PV module). This test is done first with one single long PV string impedance. It should be verified that the string voltage is Voff and the string current is loff at the starting point.						
	Test sequence	Verdict					
Step	Step	pass	fail				
1	The initiator is switched to the "normal operation" position and, after an unspecified ¹ period of time, the transmitter starts sending the keep alive signal on the PV DC line.	х	x				
2	After less than 20 seconds from the commencement of valid SunSpec KeepAlive signaling at the output of the transmitter, the receiver has completed the demodulation of the keep alive signal and connects the PV module on the DC string causing the DC						

¹ SunSpec does not specify what this time should be, but manufacturers are requested to provide an upper limit applicable to their equipment to assist testing laboratories in conducting this test. This information need not be publically disclosed.

	voltage to rise above 30V.	
3	Switch back the initiator to rapid shutdown position and restart step 1 and 2 with long string impedance and then with parallel strings impedances.	





Figure 5.1: Start Process interoperability test timing

5.2. Stop Process interoperability test: single receiver

The "start process" interoperability test is performed according the principle schematic shown in figure 4.1.

The test process is described in table 5.2 and the timing diagram is shown in figure 5.2.

Interoperability test description					
Identifier	"Rapid shutdown process" from normal operation				
Test objective	Verify that when the transmitter is in normal operation and the initiator activates a rapid shutdown, then both transmitter and receiver are working properly according to the specification. This test shall be performed with a) a single long (ZL=284 to 304μ H + DUT) and b) a single short string (ZL=11 to 14.5μ H + DUT) and c) a single short string with a long string wiring (ZL=11 to 14.5μ H + 220 μ H + DUT) and Zp corresponding to 9 parallel strings of 6 modules with an average short string wiring impedance (Zp=10 Ohm equal to 90 Ohm per string, each with max. 10% tolerance)				
Pre-test conditions	The initiator is "normal operation" position, the transmitter and the receiver are properly powered (the receiver is connected to a PV module with sun or is connected to a DC supply simulating a PV module), and the transmitter is sending the "keep alive signal. The string voltage and string current correspond to the standard operating conditions. This test is done first with a long PV string impedance.				
	Test sequence		Verdict		
Step	Step	pass	fail		
1	The initiator is switched to the "Rapid shutdown" position and after less than 4 seconds the transmitter stops sending the keep alive signal on the PV DC line.	х	х		
2	After less than 17 seconds, the receiver has completed the demodulation of the keep alive signal, the string current is loff. After less than 30 seconds, the string voltage is Voff.				
3	Switch back the initiator to normal operation position and restart step 1 and 2 with long string impedance and then with parallel strings impedances.				

Table 5.2: Stop Process interoperability test steps



Figure 5.2: Stop Process interoperability test timing

5.3. Repeated Start and Stop interoperability test: single receiver

The repeated start and stop interoperability test is performed according the principle schematic shown in figure 4.1. We propose to do this test only with long string impedance to reduce the test time and due to the fact that the long line impedance should correspond to the sensitivity level.

The test process is described in table 5.3 and the timing diagram is shown in figure 5.3.

In this test, the initiator is cyclicaly toggled between rapid shutdown position and normal operation position with the following cycle time: 1minute normal operation, 1 minute rapid shutdown position. For some specific needs, manufacturers of transmitters or receivers could specify more than 1 minute for the normal operation part of the cycle (longer re-start time).

Interoperability test description					
Identifier	"repeated Start and Stop process" interoperability test				
	Verify that the rapid shutdown mode can be activated cyclicaly and properly through a				
Test objective	minimum number of cycles (5). This test is performed with a long string (ZL=284 to 304uH)				
	The initiator is in "normal operation" position, the transmitter and the receiver are				
Dro tost	to a DC supply simulating a PV module), and the transmitter is sending the "keep alive				
	signal" The string voltage and string current correspond to the standard operating				
conditions	conditions. This test is done with a long PV string impedance ($ZL=284$ to 304 µH). The				
conditions	initiator is cyclicaly toggled between rapid shutdown position and normal operation				
	position with the following cycle time: 1minute normal operation, 1 minute rapid				
	shutdown position.				
Test sequence		Verdict			
Step	Step	pass	fail		
1	The initiator is switched to the "Rapid shutdown" position and after				
	less than 4 seconds the transmitter stops sending the keep alive	Х	Х		
	signal on the PV DC line.				
2	After less than 17 seconds, the receiver has completed the				
	demodulation of the keep alive signal, the string current is loff. After				
	less than 30 seconds, the string voltage is Voff.				
3	1 minute after rapid shutdown activation, the initiator is switched				
	back to normal operation. Both the transmitter and the receiver				
	switch back to normal operation (sending and receiving the keep				
	alive signal)				
4	Step 1 to 3 are repeated 5 times				

Table 5.3: Repeated Start and Stop process" interoperability test steps



Figure 5.3: Repeated Start and Stop process interoperability test timing

5.4. Multiple receiver interoperability test:

The principle schematic for the interoperability test with multiple receivers is shown in figure 5.4. The string voltage and combined string current are measured at the input of the transmitter (after combination of the strings). For this test, we consider 6 modules per string and an impedance of wires varying between 0uH and 220uH so the line impedance associated to each receiver is: ZL1= short PV string (11 to 14.5 μ H), ZL2 = medium PV string (140uH) and ZL3 = long PV string (304,1 μ H). We also consider that 7 other strings are connected in parallel thus presenting an impedance of approximately Zp=16 Ohms. A multiple start and stop interoperability test similar to part 5.3 is performed. The table for test steps is similar to table 5.3 (but with ZL1= 11 to 14.5 μ H, ZL2=140uH, ZL3=304 μ H, Zp=16 Ohms) and the timing diagram is similar to figure 5.3 (but with "combined loff" instead of loff).



Figure 5.4: Multiple Receiver interoperability test diagram

APPENDIX A: Signal Timing and Waveform Accuracy

Informative: MATLAB CODE FOR SIGNAL TIMING AND WAVEFORM ACCURACY ASSESSMENT

The following MATLAB® script is an illustrative example of one possible approach to implementing the normative signal processing steps used for assessing SunSpec RSD keep-alive waveform accuracy and timing. Use of this code, or parts thereof, does not imply a correct implementation of any part of the official SunSpec test procedure.

```
%% read signal from file
load 'tx capture.mat'% loads a vector named "signal"
Fs=2e6;
           % sample rate, must match input tx_capture sample rate.
Tb=5.12e-3; % bit duration
bits per codeword=11;
codewords per period=19;
samples per period=round(codewords per period*bits per codeword*Tb*Fs);
%% compute bit waveform
N=round(Fs/6250); %filter length
assert(N*6250==Fs, Sample rate not a multiple of the tone spacing');
bitwave=abs(filter(2*exp(1i*2*pi*21*(0:1/N:1-1/N))/N,1,signal)) - ...
       abs(filter(2*exp(1i*2*pi*23*(0:1/N:1-1/N))/N,1,signal));
%% define ideal reference for correlation searches
barker=[-1 -1 -1 1 1 1 -1 1 1 -1 1];
ref=kron(repmat(barker,1,3),ones(1,round(Fs*Tb)));
ref=ref/norm(ref); % normalize
%% find correlation peaks and their timing
Nexpected=floor(length(bitwave)/samples_per_period);
% truncate to integer number of duty-cycle periods
bitwave=bitwave(1:samples per period*Nexpected)';
bitwave=sqrt(Nexpected)*bitwave/norm(bitwave); %normalize
ref=[ref, zeros(1,length(bitwave)-length(ref))]; % zero-pad
% circular cross-correlation using FFT method
xcorr1=ifft((fft(bitwave)).*conj(fft((ref))));
[pks,locs]=findpeaks(abs(xcorr1), 'MinPeakHeight',0.9,...
```

```
'MinPeakWidth',0,'MinPeakDistance',0);
[locs,i]=sort(locs);
pks=pks(i);
num_peaks=length(pks);
assert(num_peaks==Nexpected,'number of peaks found was not correct');
%% print a formatted table of results
actual_times=(locs-locs(1))/Fs;
ideal_times=(0:num_peaks-1)*codewords_per_period*bits_per_codeword*Tb;
ppm=1E6*(actual_times - ideal_times)./(ideal_times+eps);
T=[ideal_times',actual_times',pks',ppm'];
fprintf(1,'%s\t%s\t%s\t%s\t%s\t%s\t%s\t%s\t%t\t\t%4.1f\n',T');
```

APPENDIX B: Simulating Additional Receiver or Parallel Strings

Informative: Simulating additional receivers or parallel strings for the interoperability test

Simulating additional receiver in one string

In Table 6 of [1], the impedance of one receiver is specified to 0.7 to 1.5 Ohms. The attached wiring of a typical PV-Module is in the range of two times 0.9 m. In a best practice PV System the go and return line will be drilled to achieve a low inductance. A pair of 0.9m drilled PV wiring equates to approximately 1.3 μ H additional inductance. To simulate one PV module with an added receiver simplified by an inductance, the impedance of the receiver has to be mapped to a corresponding inductance value: 0.7 Ohm @ 131.3 kHz = 0.9 μ H; 1.5Ohm @ 143.8kHz = 1.6 μ H. Adding both values - wiring and receiver impedance - results in **2.2\muH to 2.9\muH per simulated PV module including its attached module wiring.**

Example: If one string composed of 6 modules in sum should be emulated by one DUT together with an inductance in series, the value of the inductance shall be in the range of 5 x (2.2μ H to 2.9μ H) = 11 to 14.5 μ H. To simulate the addition of PV DC-Power or a standby signal, a power supply has to also be added in series.

Simulating additional wiring in one string

To simulate the additional wiring from the PV array to the inverter, an additional inductance has to be added in series or the value of an existing inductance has to be increased. This specification covers up to **220 µH** of extra wiring in addition to the PV module attached wiring.

Example: If one string composed of 30 modules in sum with additional very long wiring to the inverter should be emulated by one DUT together with an inductance in series, the value of the inductance shall be in the range of 29 x (2.2μ H to 2.9μ H) + 220μ H = 283,8 to 304,1 μ H. To simulate the addition of DC-Power or Standby Voltage a power supply has to be added in series too.

Simulating additional parallel strings

To simulate an entire parallel string without any DUT in series of this parallel string, an RC series circuit shall be used. The appropriate values are: 1.3 μ H @ 131.3 kHz = 1.1 Ohm for the PV module attached wiring plus the receiver impedance of 0.7 to 1.5 Ohm \rightarrow **1.8 Ohm to 2.6 Ohm** per simulated PV module including its attached module wiring. To simulate the additional wiring from the PV array to the inverter, an additional resistance of up to **200 Ohm** shall be used (~220 μ H @ 143.8 kHz). The used capacitor shall be >= 1 μ F per simulated string.

Example: If one string composed of 30 modules in sum with additional very long wiring to the inverter should be emulated without any DUT to this, a resistance in the range of 30 x 1.8 Ohm to 2.6 Ohm + 200Ohm = 254 to 278 Ohm together with a capacitor of >= 1μ F in series must be added in parallel to the existing test setup.